Electronic Version
Stylesheet Version v1.1.1

Description

METHOD FOR CODING SEMICONDUCTOR PERMANENT STORE ROM

BACKGROUND OF INVENTION

[0001] 1. Field of the Invention

[0002] The present invention relates generally to a method for manufacturing read only memory (ROM) devices. More specifically, a method is disclosed for shortening the product turn-around time for making semiconductor permanent store ROM by ROM coding the memory in a late stage. Instead of threshold voltage implantation, the present invention uses deep trench etching to implement ROM cell coding.

[0003] 2. Description of the Prior Art

[0004] Read-only memory (ROM), also known as firmware, is an integrated circuit programmed with specific data when it is manufactured. ROM chips are used not only in comput-

ers, but in most other electronic items as well. The process of programming data is also referred to as coding. Hitherto, numerous coding methods have been developed to program data into the memory cells during different phases of their manufacture. One development that has gained wide use is the threshold voltage implant method, which changes a transistor"s threshold voltage by ion implanting the transistor gates for programmed cells. By way of example, for coding an N-channel memory cell, a predetermined dosage of impurities such as boron are implanted into the channel area under the gate of the transistor to raise its threshold voltage, thereby turning this memory cell into an "off" state. Another coding method includes selectively opening the contact holes for each transistor to drain. Such method, which is also known as the through-hole contact programming technique, requires a contact for every cell, thereby increasing the size of the cell array.

[0005] It is often desirable to apply the ROM code onto the partially completed devices during a latter part of the manufacturing process. By applying the code at the latter part of the process, it takes less time to complete wafer processing. Customers require the product turn-around time

between reception of the ROM code for a custom order and delivery of finished parts to be kept as short as possible. Less time for completion means a shorter product turn-around time.

[0006] U.S. Pat. No. 4,268,950, filed June 5, 1978 by Chatterjee et al., assigned to Texas Instruments discloses a process for making an N-channel silicon gate MOS read only memory that may be programmed at a late stage in the manufacturing process. The cell array is programmed by boron implantation through a protective nitride, polysilicon strips, and gate oxides to raise the threshold voltage of selected cells to a value above that which will be turned on by the voltage on the selected address line. U.S. Pat. No. 5,514,609, filed May 13, 1994 by Chen et al., assigned to Mosel Vitelic discloses the manufacture of a ROM cell that is coded before metallization. ROM code impurities are implanted first through a dielectric layer overlying gate electrodes, and then through the underlying selected gate electrodes.

[0007] U.S. Pat. No. 6,020,241, filed December 22, 1997 by You et al., assigned to Taiwan Semiconductor Manufacturing Company discloses a method of manufacturing a ROM that is code implanted late in the process after the first

level metal thus reducing the turn-around time to ship a customer order. The code implantation implants impurities through a first dielectric layer overlying gates and a second dielectric layer overlying the first dielectric layer, and through a portion of the word lines.

SUMMARY OF INVENTION

[0008] It is therefore a primary objective of this invention to provide a method for manufacturing high-density read only memory (ROM) devices, thereby shortening the product turn-around time.

[0009] Briefly summarized, the preferred embodiment of the present invention discloses a method for manufacturing a read only memory (ROM) device capable of shortening product turn-around time. A semiconductor substrate having thereon an array of metal-oxide-semiconductor field-effect transistors (MOSFETs) within a ROM region is provided. A dielectric layer covers the MOSFETs within the ROM region. Each of the MOSFETs has a gate, a source, and a drain. All of the MOSFETs are initially in an "ON" state. The method comprises forming a coding photoresist layer on the dielectric layer. The coding photoresist layer is then patterned to form a plurality of apertures defining exposure windows where the underlying MOS-

FETs are to be coded from the "ON" state into an "OFF" state. The exposure windows are disposed above the sources of the MOSFETs to be coded. An etching process is carried out, using the patterning coding photoresist layer as an etching hard mask, to etch the dielectric layer, the sources of the MOSFETs to be coded, and a portion of the semiconductor substrate underneath the sources of the MOSFETs to be coded through the exposure windows to a depth that is lower than a junction depth of the sources of the MOSFETs to be coded, to form a deep trench that disconnects the sources of the MOSFETs to be coded from source lines. The coding photoresist layer is stripped. A gap fill layer is deposited over the dielectric layer to fill the deep trench.

[0010] According to the claimed invention, a method for manufacturing a read only memory (ROM) device is disclosed. A semiconductor substrate having thereon an array of field-effect transistors within a ROM region and a first dielectric layer covering the array of field-effect transistors is provided. Each of the MOSFETs has a gate, a drain, and a source connected to a source line. All of the field-effect transistors are initially in an "ON" state. The method comprises forming bit lines on the first dielectric layer within

the ROM region. The bit lines are covered by a second dielectric layer. The bit lines bypass the underlying sources of the array of the field-effect transistors to not overlap with the sources. A coding photoresist layer is formed on the second dielectric layer. The coding photoresist layer is then patterned to form a plurality of apertures defining exposure windows where the underlying field-effect transistors are to be coded permanently to an "OFF" state. A code etching back process is implemented using the patterning coding photoresist layer as an etching hard mask to etch the second dielectric layer, the first dielectric layer, the sources of the MOSFETs to be coded, and a portion of the semiconductor substrate underneath the sources of the MOSFETs to be coded through the exposure windows to a depth that is lower than a junction depth of the sources of the MOSFETs to be coded, so as to form a deep trench, which disconnects the sources of the MOSFETs to be coded from the source lines. The coding photoresist layer is stripped. A gap fill layer is thereafter deposited over the dielectric layer to fill the deep trench.

[0011] Other objects, advantages, and novel features of the claimed invention will become more clearly and readily apparent from the following detailed description when

taken in conjunction with the accompanying drawings.

Brief Description of Drawings

[0012] The accompanying drawings are included to provide a further understanding of the invention, and are incorporated in and constitute a part of this specification. The drawings illustrate embodiments of the invention and, together with the description, serve to explain the principles of the invention. In the drawings:

[0013] Fig.1 illustrates a portion of a ROM array, which is programmed according to this invention.

[0014] Fig.2 to Fig.8 are schematic cross-sectional diagrams illustrating the first preferred embodiment according to the present invention.

[0015] Fig.9 is an enlarged top view of the cell to be coded and the window thereof as set forth in Fig.4.

[0016] Fig.10 to Fig.15 are schematic cross-sectional diagrams illustrating the second preferred embodiment according to the present invention.

[0017] Fig.16 is an enlarged top view depicting the special bit line pattern within the ROM section of Fig.12.

[0018] Fig.17 is an enlarged top view of the cell to be coded and the window thereof as set forth in Fig.13.

Detailed Description

[0019] The preferred embodiment in accordance with the present invention will be discussed in detail with reference to Fig.1to Fig.17. It is understood that the type of semiconductor regions, device layout, and polarity of voltages are chosen solely for illustration, and persons having ordinary skill in the art would recognize other alternatives, variations, and modifications.

[0020] Please refer to Fig.1. Fig.1 illustrates a portion of a ROM array, which is programmed according to this invention. The ROM array consists of a large number of memory cells, only four of which are shown for simplicity. As shown in Fig.1, the exemplary four memory cells are cell (0,0), cell (0,1), cell (1,0), and cell (1,1). Each cell is a MOS transistor having a gate 10, a drain 12, and a source 14. The gates 10 are parts of word lines WL_0, WL_1, which are the X address lines for the array. The drains 12, which are N^+ diffusion regions, are electrically connected to bit lines (or Y output lines) BL_0, BL_1. The sources 14 are N^+ diffusion regions, which are defined along with the drains 12. According to the present invention, the specific binary code is programmed into the ROM array through a source-side code mask and an etching back process. As indicated, the source 14 of the cell (0,0) is disconnected

from the corresponding source line to store logic data "1". The other cells storing logic data "0" have the sources 14 electrically connected to the source lines (not shown) that are grounded or biased to Vss.

[0021] With reference to Fig.2 to Fig.8, a first preferred embodiment according to the present invention is illustrated in cross-sectional views. As shown in Fig.2, a semiconductor substrate 200 is provided having a main surface on which a plurality of MOS transistors 101, 102, and 201 are formed. The main surface of the semiconductor substrate 200 is basically divided into two sections: the ROM section 301 and the peripheral section 302. An array of memory cells is formed within the ROM section 301, and only cells 101 and 102 are shown. The MOS transistor 201, which may be an active device of the peripheral circuit, is formed within the peripheral section 302. Each MOS transistor within the ROM section 301 has a gate 401, a drain 402, and a source 403. The gates 401 are parts of word lines or X address lines. The sources 403 are electrically connected to the source lines (not shown) that are grounded or biased to Vss. As shown in Fig.3, a dielectric layer 501 such as an LPCVD silicon oxide layer or a BPSG layer is deposited overlying the ROM section 301 and the peripheral

section 302. Preferably, the dielectric layer 501 has a thickness of between 2000 and 7000 angstroms.

[0022] As shown in Fig.4, a coding photoresist layer 601 is coated on the dielectric layer 501. The coding photoresist layer 601 is exposed to ultraviolet (UV) light through a photo mask that defines the customer ROM code. After development, the unexposed coding photoresist layer 601 is removed leaving a plurality of apertures defining exposure windows where the underlying memory cells within the ROM section 301 are to be coded permanently to an "OFF" state. In this case, the cell 102 is chosen, by way of example, as the transistor to be coded to an "OFF" state and only one window 611 is illustrated. It is noted that, at this phase, the peripheral section 301 is still masked by the coding photoresist layer 601. Referring to Fig.9, a planar view showing the cell 102 and window 611 of Fig.4 is illustrated. The length L of the window 611 must be greater than the width W of the source 403 of the transistor 102 to be coded.

[0023] As shown in Fig.5, using the coding photoresist layer 601 as a etching mask, an etching back process is carried out to etch the dielectric layer 501, the source 403 of the transistor 102, and a portion of the substrate 200 under-

neath the source 403 of the transistor 102 through the window 611 to a depth that is lower than the junction depth of the source of the transistor 102, so as to form a deep trench 711. That is, the depth of the deep trench 711 is larger than the combination of the thickness of the dielectric layer 501 and the junction depth of the source 403 of the transistor 102 for storing logic data "1". By doing this, the source 403 of the transistor 102 for storing logic data "1" is disconnected from the source line. As shown in Fig.6, after stripping the coding photoresist layer 601, a gap fill layer 701 is deposited over the dielectric layer 501 to fill the deep trench 711.

[0024] As shown in Fig.7, in accordance with the first preferred embodiment of the present invention, after coding the ROM section 301, metallization is carried out. A photoresist layer 801 is coated on the gap fill layer 701 and patterned to form openings 811 that define the location of contact holes within the ROM section 301 and the peripheral section 302. An etching process is then implemented to etch the gap fill layer 701 and the dielectric layer 501 to expose portions of the underlying drains 402 through the openings 811 to form contact holes 911. The following metallization processes including contact plug forma-

tion and metal line patterning are known in the art and are thus omitted.

[0025] With reference to Fig.10 to Fig.15, a second preferred embodiment according to the present invention is illustrated in cross-sectional views in which like reference numerals designate similar or corresponding elements, regions, and portions. As shown in Fig.10, a semiconductor substrate 200 is provided having a main surface on which a plurality of MOS transistors 101, 102, and 201 are formed. Likewise, the main surface of the semiconductor substrate 200 is basically divided into two sections: the ROM section 301 and the peripheral section 302. An array of memory cells is formed within the ROM section 301, and only cells 101 and 102 are shown. The MOS transistor 201, which may be an active device of the peripheral circuit, is formed within the peripheral section 302. Each MOS transistor within the ROM section 301 has a gate 401, a drain 402, and a source 403. The gates 401 are parts of word lines or X address lines. The sources 403 are electrically connected to the source lines (not shown) that are grounded or biased to Vss.

[0026] As shown in Fig.11, a dielectric layer 501 such as an LPCVD silicon oxide layer or a BPSG layer is deposited

overlying the ROM section 301 and the peripheral section 302. Preferably, the dielectric layer 501 has a thickness of between 2000 and 7000 angstroms.

[0027] As shown in Fig.12, metallization is carried out. Within the peripheral section 302, multi-level metal lines and connecting contacts or vias are formed. As indicated, a contact C_1 is formed in the dielectric layer 501 to connect the source or drain of the transistor 201 with the first level metal M_1. The first level of metal within the ROM section 301 is patterned to form a bit line BL overlying the dielectric layer 501. The bit line BL is electrically connected to the drains 402 of the underlying MOS transistors 101 and 102 through the contact C_2 formed in the dielectric layer 501. Referring to Fig.16, a top view depicting the special bit line pattern within the ROM section 301 of Fig.12 is illustrated. The bit lines basically overlie the word line in an orthogonal manner, but bypass the underlying source regions 403 to not overlap the source regions 403. After forming the first level metal lines, a second level metal line M_2 is defined within the peripheral section 302 over an inter-metal dielectric (IMD) layer 502. The second level metal line M_2 is electrically connected to the first level metal through the via V_1, which is formed in the IMD layer

502. The IMD layer 502 also covers the bit line BL within the ROM section 301. After finishing the metalization processes, a passivation layer 503 is deposited on the second level metal line M_2, and on the IMD layer 502 within the ROM section 301 and the peripheral section 302. After this, the semiconductor device is stored or "banked". The device is held awaiting the details of a custom"s order, which will determine the exact configuration of the code implant.

[0028] As shown in Fig.14, a coding photoresist layer 601 is coated on the dielectric layer 501. The coding photoresist layer 601 is exposed to ultraviolet (UV) light through a photo mask that defines the customer ROM code. After development, the unexposed coding photoresist layer 601 is removed leaving a plurality of apertures defining exposure windows where the underlying memory cells or transistors within the ROM section 301 are to be coded permanently to an "OFF" state. In this case, the cell 102 is chosen, by way of example, as the transistor to be coded to an "OFF" state and only one window 611 is illustrated. Referring to Fig.17, a planar view showing the cell 102 and window 611 of Fig.14 is illustrated.

[0029] As shown in Fig.14, using the coding photoresist layer

601 as a etching mask, an etching back process is carried out to etch the passivation layer 503, the IMD layer 502, the dielectric layer 501, the source 403 of the transistor 102, and a portion of the substrate 200 underneath the source 403 of the transistor 102 through the window 611 to a depth that is lower than the junction depth of the source 403 of the transistor 102 to form a deep trench 711. The depth of the deep trench 711 is larger than the combination of the thickness of the passivation layer 503, the IMD layer 502, the dielectric layer 501 and the junction depth of the source 403 of the transistor 102 for storing logic data "1". By doing this, the source 403 of the transistor 102 for storing logic data "1" is disconnected from the source line. As shown in Fig.15, after stripping the coding photoresist layer 601, a gap fill layer 701 is deposited over the passivation layer 503 to fill the deep trench 711. As mentioned, customers require the product turn-around time between reception of the ROM code for a custom order and delivery of finished parts to be kept as short as possible. Less time for completion means a shorter product turn-around time. Coding after metallization can minimize the product turn-around time.

[0030] Those skilled in the art will readily observe that numerous

modifications and alterations of the present invention method may be made while retaining the teachings of the invention. Accordingly, the above disclosure should be construed as limited only by the metes and bounds of the appended claims.